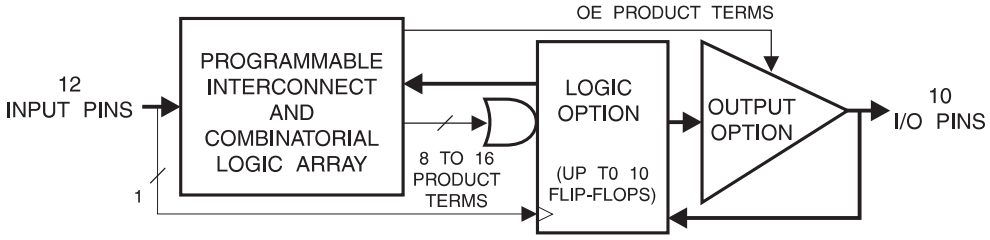
Features

- **Industry Standard Architecture**
  - **Low Cost Easy-to-Use Software Tools**
- **High Speed Electrically Erasable Programmable Logic Devices**
  - **5 ns Maximum Pin-to-Pin Delay**
- **CMOS and TTL Compatible Inputs and Outputs**
  - **Latch Feature Holds Inputs to Previous Logic States**
- **Advanced Flash Technology**
  - **Reprogrammable**
  - **100% Tested**
- **High Reliability CMOS Process**
  - **20 Year Data Retention**
  - **100 Erase/Write Cycles**
  - **2,000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Dual-in-Line and Surface Mount Packages in Standard Pinouts**

High Performance E^2 PLD

ATF22V10C

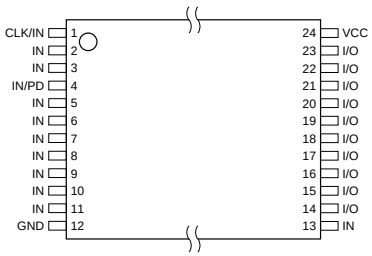
Logic Diagram



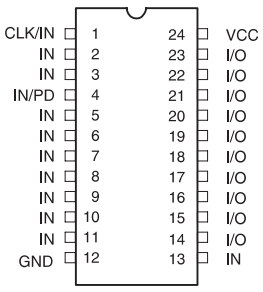
Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
*	No Internal Connection
VCC	+5V Supply
PD	Power Down

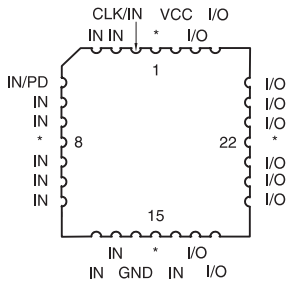
TSSOP Top View



DIP/SOIC



PLCC



Top view

Note: For PLCC, pins 1, 8, 15 and 22 can be left unconnected. For superior performance, connect V_{CC} to pin 1 and ground to 8, 15, 22.

Rev. 0735C/22V10C-D–04/98

Description

The ATF22V10C is a high performance CMOS (Electrically Erasable) Programmable Logic Device (PLD) which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 5 ns and power dissipation as low as 100 µA are offered. All speed ranges are specified over the full 5V ± 10% range for industrial temperature ranges, and 5V ± 5% for commercial temperature ranges.

Several low power options allow selection of the best solution for various types of power-limited applications. Each of these options significantly reduces total system power and enhances system reliability.

Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V (1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V (1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V (1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6V dc, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc, which may overshoot to 7.0V for pulses of less than 20 ns.

DC and AC Operating Conditions

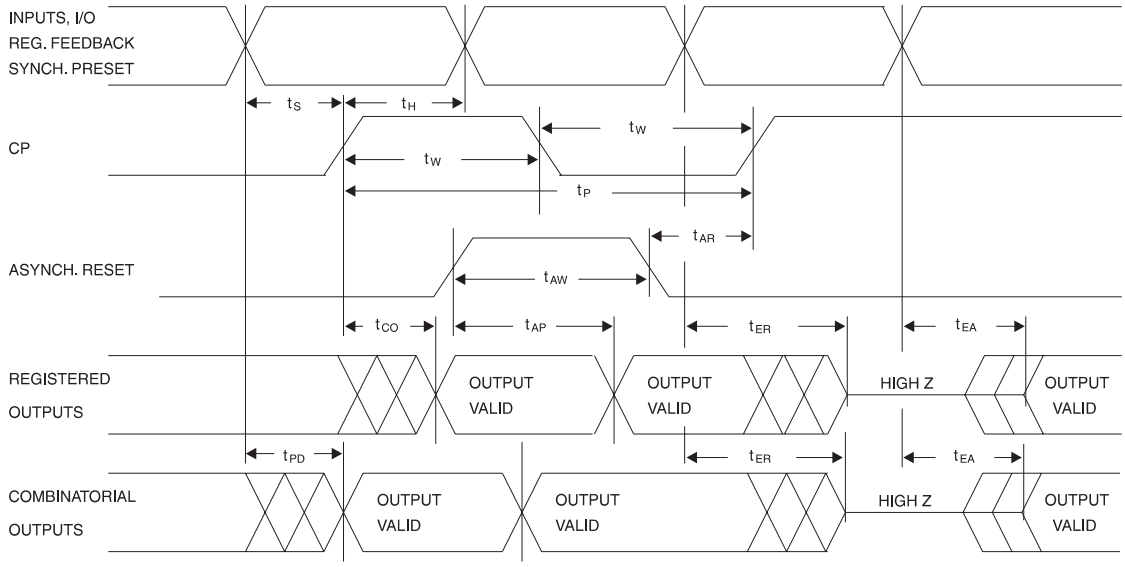
	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	5V ± 5%	5V ± 10%

DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$(MAX)				-35	-10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$					10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = MAX, V_{IN} = MAX, Outputs Open	C-5, 7, 10	Com.		85	130	mA
			C-10	Ind.		90	140	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open	C-5, 7, 10	Com.		1		mA/MHz(2)
			C-10	Ind.		1		mA/MHz(2)
I_{CC3}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open, f = 15 MHz	C-5, 7, 10	Com.			150	mA
			C-10	Ind.			160	mA
I_{PD}	Power Supply Current, PD Mode	V_{CC} = MAX		Com.		10	100	µA
		V_{IN} = 0, MAX		Ind.		10	100	µA
I_{OS}(1)	Output Short Circuit Current	V_{OUT} = 0.5V					-130	mA
V_{IL}	Input Low Voltage				-0.5		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = MIN	I_{OL} = 16 mA	Com., Ind.			0.5	V
			I_{OL} = 12 mA	Mil.			0.5	V
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = MIN	I_{OH} = -4.0 mA		2.4			V

Notes: 1. Not more than one output at a time should be shorted.
Duration of short circuit test should not exceed 30 sec.
2. Low frequency only. See Supply Current versus Input Frequency curves.

AC Waveforms (1)



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

AC Characteristics (1)

Symbol	Parameter	-5		-7		-10		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output	1	5	3	7.5	3	10	ns
t_{CO}	Clock to Output	1	4	2	4.5 (2)	2	6.5	ns
tCF	Clock to Feedback		3		3.5		4	ns
tS	Input or Feedback Setup Time	3		3.5		4.5		ns
t_H	Hold Time	0		0		0		ns
F_{MAX}	External Feedback $1/(t_S + t_{CO})$		142		125 (3)		90	MHz
	Internal Feedback $1/(t_S + t_{CF})$		166		142		117	MHz
	No Feedback		166		166		125	MHz
t_P	Clock Period	6		6		8		ns
t_W	Clock Width	3		3		3		ns
t_{EA}	Input or I/O to Output Enable	2	6	3	7.5	3	10	ns
t_{ER}	Input or I/O to Output Disable	2	5	3	7.5	3	9	ns
t_{AP}	Input or I/O to Asynchronous Reset of Register	3	7	3	10	3	12	ns
t_{AW}	Asynchronous Reset Width	5.5		7		8		ns
t_{AR}	Asynchronous Reset Recovery Time	4		5		6		ns
t_{SP}	Setup Time, Synchronous Preset	4		4.5		6		ns
t_{SPR}	Synchronous Preset to Clock Recovery Time	4		5		8		ns

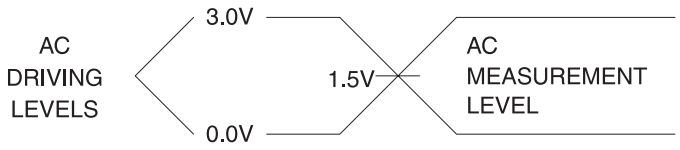
Notes: 1. See ordering information for valid part numbers.
2. 5.5 ns for DIP package devices.
3. 111 MHz for DIP package devices.

Power Down AC Characteristics (1, 2, 3)

Symbol	Parameter	-5		-7		-10		Units
		Min	Max	Min	Max	Min	Max	
t_{IVDH}	Valid Input Before PD High	5		7.5		10		ns
t_{GVDH}	Valid $\overline{OE}$ Before PD High	0		0		0		ns
t_{CVDH}	Valid Clock Before PD High	0		0		0		ns
t_{DHIX}	Input Don't Care After PD High		5		7		10	ns
t_{DHGX}	$\overline{OE}$ Don't Care After PD High		5		7		10	ns
t_{DHCX}	Clock Don't Care After PD High		5		7		10	ns
t_{DLIV}	PD Low to Valid Input		5		7.5		10	ns
t_{DLGV}	PD Low to Valid $\overline{OE}$		15		20		25	ns
t_{DLCV}	PD Low to Valid Clock		15		20		25	ns
t_{DLOV}	PD Low to Valid Output		20		25		30	ns

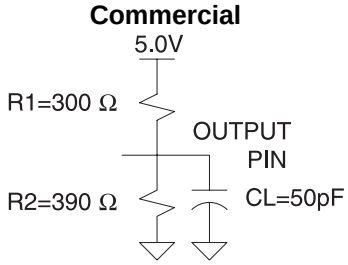
Notes: 1. Output data is latched and held.
2. HI-Z outputs remain HI-Z.
3. Clock and input transitions are ignored.

Input Test Waveforms and Measurement Levels



t_R, t_F < 3 ns

Output Test Loads:



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
C_{OUT}	6	8	pF	V_{OUT} = 0V

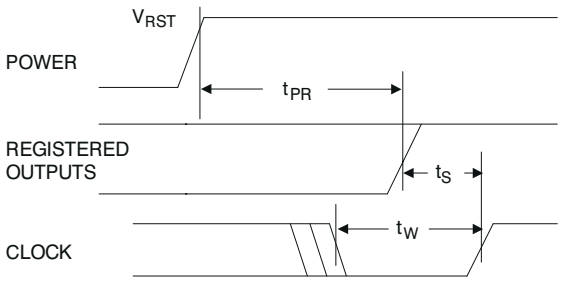
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power Up Reset

The registers in the ATF22V10Cs are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic, and starts below 0.7V,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and
3. The clock must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-Up Reset Time	600	1,000	ns
V_{RST}	Power-Up Reset Voltage	3.8	4.5	V

Preload of Registered Outputs

The ATF22V10C's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF22V10C fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

Electronic Signature Word

There are 64 bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

Programming/Erasing

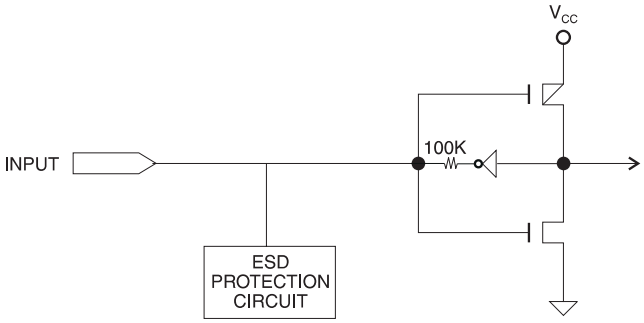
Programming/erasing is performed using standard PLD programmers. See *CMOS PLD Programming Hardware & Software Support* for information on software/programming.

Input and I/O Pin Keeper Circuits

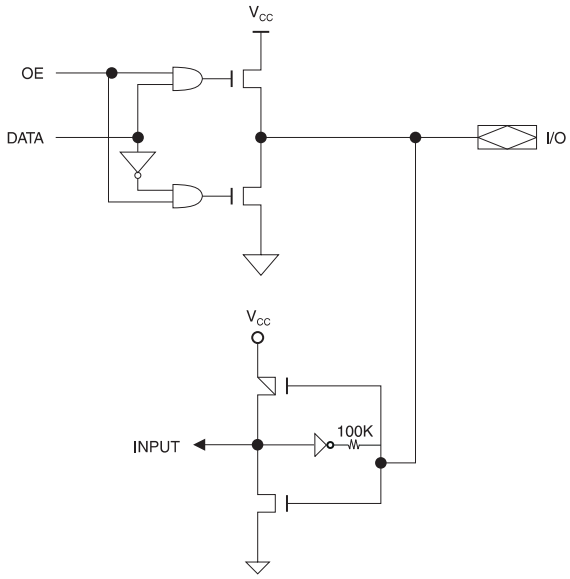
The ATF16V8C contains internal input and I/O pin keeper circuits. These circuits allow each ATF16V8C pin to hold its previous value even when it is not being driven by an external source or by the device's output buffer. This helps insure that all logic array inputs are at known, valid logic levels. This reduces system power by preventing pins from floating to indeterminate levels. By using pin keeper circuits rather than pull-up resistors, there is no DC current required to hold the pins in either logic state (high or low).

These pin keeper circuits are implemented as weak feedback inverters, as shown in the Input Diagram below. These keeper circuits can easily be overdriven by standard TTL- or CMOS-compatible drivers. The typical overdrive current required is 40 µA.

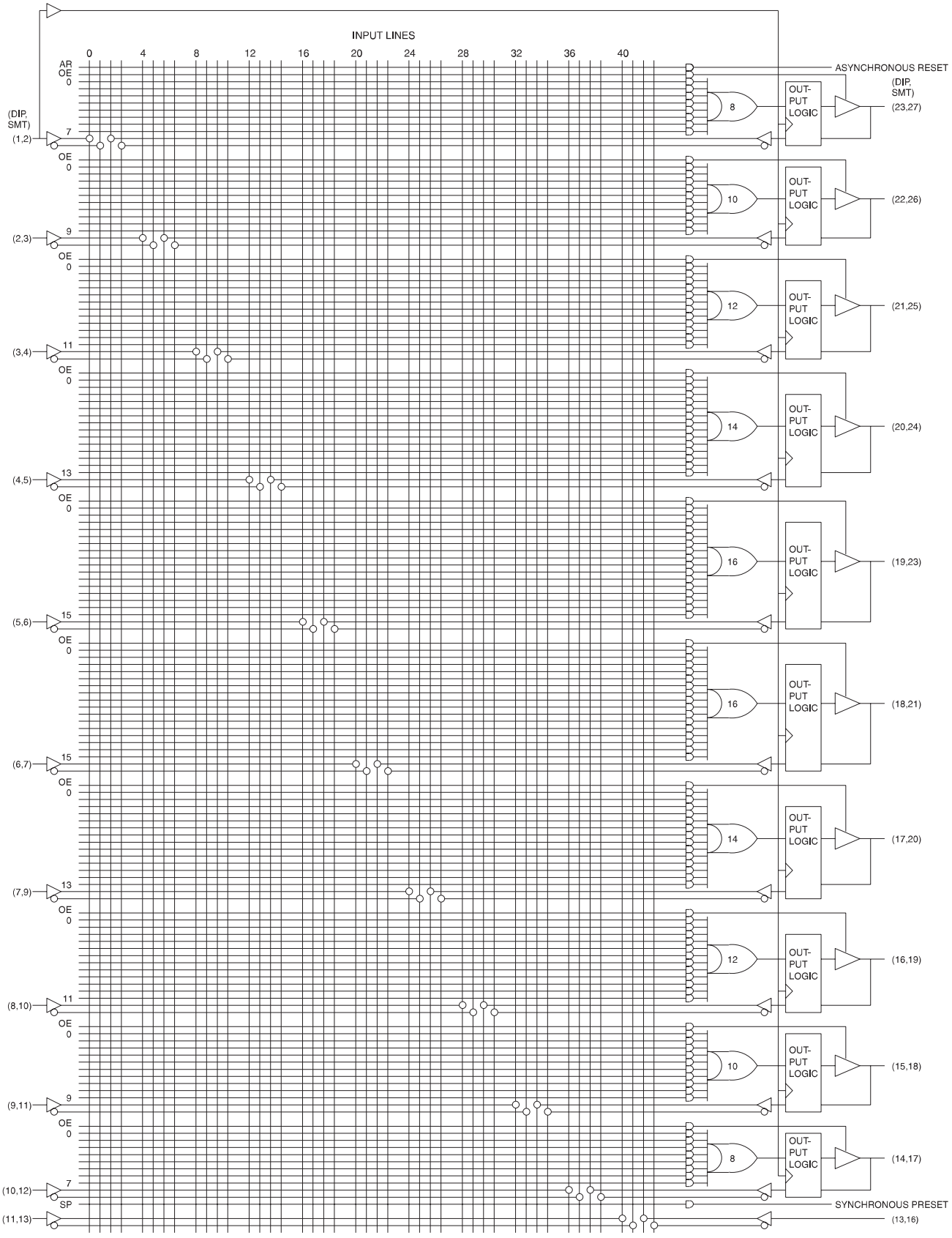
Input Diagram



I/O Diagram



Functional Logic Diagram ATF22V10C



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
5	3	4	ATF22V10C-5JC	28J	Commercial (0°C to 70°C)
7.5	3.5	4.5	ATF22V10C-7JC ATF22V10C-7PC ATF22V10C-7SC ATF22V10C-7XC	28J 24P3 24S 24X	Commercial (0°C to 70°C)
10	4.5	6.5	ATF22V10C-10JC ATF22V10C-10PC ATF22V10C-10SC ATF22V10C-10XC	28J 24P3 24S 24X	Commercial (0°C to 70°C)
			ATF22V10C-10JI ATF22V10C-10PI ATF22V10C-10SI ATF22V10C-10XI	28J 24P3 24S 24X	Industrial (-40°C to 85°C)

Package Type	
28J	28-Lead, Plastic J-Leaded Chip Carrier (PLCC)
24P3	24-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
24S	24-Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
24X	24-Lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)